Claims

1. A method for forming an integrated circuit comprising the steps of:

providing a substrate having a center and a perimeter;

forming a layer of material overlying the substrate;

providing a polishing pad having a perimeter and a center, the polishing pad comprising a first polishing region, a second polishing region, and a third polishing region, wherein the second polishing region lies between the first polishing region and the third polishing region;

aligning the substrate to the polishing pad such that the center of the substrate overlies the second polishing region, a first portion of the perimeter of the substrate overlies the first polishing region, and a second portion of the perimeter of the substrate overlies the third polishing region; and

polishing the layer of material overlying the substrate using the polishing pad, wherein the center of the substrate remains at a fixed distance from the perimeter of the polishing pad while the layer of material is polished.

2. The method of claim 1, wherein the first polishing region has a first hole density, the second polishing region has a second hole density, and the third polishing region has a third hole density.

3. The method of claim 2, wherein the second hole density is greater than the first hole density and the third hole density.

4. The method of claim 1, wherein the first polishing region comprises a first plurality of holes having a first hole depth and a first hole width, the second polishing region comprises a second plurality of holes having a second hole depth and a second hole width, and the third polishing region comprises a third plurality of holes having a third hole depth and a third hole width.

5. The method of claim 4, wherein the second hole depth is greater than the first hole depth and the third hole depth.

6. The method of claim 4, wherein the second hole width is greater than the first hole width and the third hole width.

7. The method of claim 1, wherein the first polishing region has a first pore density, the second polishing region has a second pore density, and the third polishing region has a third pore density.

8. The method of claim 7, wherein the second pore density is greater than the first pore density and the third pore density.

9. The method of claim 1, wherein the layer of material comprises a dielectric layer.

10. The method of claim 9, wherein the step of polishing the layer of material is further characterized as polishing the layer of material to form a trench isolation region.

11. The method of claim 9, wherein the step of polishing the layer of material is further characterized as polishing the layer of material to form a planarized interlevel dielectric layer.

12. The method of claim 1, wherein the layer of material comprises a conductive layer.

13. The method of claim 12, wherein the step of polishing the layer of material is further characterized as polishing the layer of material to form a conductive interconnect.

14. A method for forming an integrated circuit comprising the steps of:

providing a substrate having a center and a perimeter;

forming a layer of material overlying the substrate;

providing a polishing pad having a perimeter and a center, the polishing pad comprising a first polishing region, a second polishing region, and a third polishing region, wherein the second polishing region lies between the first polishing region and the third polishing region;

using an alignment detector to align the substrate to the second polishing region of the polishing pad, such that the center of the substrate overlies the second polishing region, a first portion of the perimeter of the substrate overlies the first polishing region, and a second portion of the perimeter of the substrate overlies the third polishing region; and

polishing the layer of material overlying the substrate using the polishing pad, wherein the center of the substrate remains at a fixed distance from the perimeter of the polishing pad while the layer of material is polished.

15. The method of claim 14, wherein the first polishing region has a first hole density, the second polishing region has a second hole density, and the third polishing region has a third hole density.

16. The method of claim 15, wherein the second hole density is greater than the first hole density and the third hole density.

17. The method of claim 14, wherein the first polishing region comprises a first plurality of holes having a first hole depth and a first hole width, the second polishing region comprises a second plurality of holes having a second hole depth and a second hole width, and the third polishing region comprises a third plurality of holes having a third hole depth and a third hole width.

18. The method of claim 17, wherein the second hole depth is greater than the first hole depth and the third hole depth.

19. The method of claim 17, wherein the second hole width is greater than the first hole width and the third hole width.

20. The method of claim 14, wherein the first polishing region has a first pore density, the second polishing region has a second pore density, and the third polishing region has a third pore density.

21. The method of claim 20, wherein the second pore density is greater than the first pore density and the third pore density.

22. The method of claim 14, wherein the alignment detector comprises a laser.

23. The method of claim 14, wherein the alignment detector comprises a video camera.

24. The method of claim 14, wherein the layer of material is further characterized as a copper layer.

25. The method of claim 24, further comprising the step of dispensing a slurry comprising hydrogen peroxide on the polishing pad.

26. The method of claim 14, wherein the layer of material is further characterized as a tungsten layer.

27. The method of claim 26, further comprising the step of dispensing a slurry comprising ferric nitrate on the polishing pad.

28. The method of claim 14, wherein the layer of material is further characterized as a silicon oxide layer.

29. The method of claim 28, further comprising the step of dispensing a slurry comprising potassium hydroxide on the polishing pad.

30. A polishing apparatus comprising:

a polishing platen;

a polishing pad overlying the polishing platen, the polishing pad having a first polishing region, a second polishing region, and a third polishing region, wherein the second polishing region lies between the first polishing region and the second polishing region;

a carrier; and

an alignment detector, wherein the alignment detector is used to align the carrier to the second polishing region of the polishing pad.

31. The polishing apparatus of claim 30, wherein the polishing platen is further characterized as having an alignment knob.

32. The polishing apparatus of claim 30, wherein the alignment detector comprises a laser.

33. The polishing apparatus of claim 30, wherein the alignment detector comprises a video camera.

34. The polishing apparatus of claim 30, wherein the first polishing region has a first hole density, the second polishing region has a second hole density, and the third polishing region has a third hole density.

35. The polishing apparatus of claim 34, wherein the second hole density is greater than the first hole density and the third hole density.

36. The polishing apparatus of claim 30, wherein the first polishing region comprises a first plurality of holes having a first hole depth and a first hole width, the second polishing region comprises a second plurality of holes having a second hole depth and a second hole width, and the third polishing region comprises a third plurality of holes having a third hole depth and a third hole width.

37. The polishing apparatus of claim 36, wherein the second hole depth is greater than the first hole depth and the third hole depth.

38. The polishing apparatus of claim 36, wherein the second hole width is greater than the first hole width and the third hole width.